# ULAs 8

## High Speed CMOS Uncommitted Logic Arrays (ULAs)



| FUNCTION | DESCRIPTION | PART NUMBER | PAGE NUMBER |
|---|---|---|---|
| | | **Uncommitted Logic Arrays** | |
| HIGH SPEED CMOS UNCOMMITTED LOGIC ARRAYS | Single mask, 5ns gate delay, single supply voltage, CMOS technology, on-chip power-on reset. | LA03 | 8-3 |
| | | LA05 | 8-3 |
| | | LA10 | 8-3 |
| | | LA15 | 8-3 |
| | | LA20 | 8-3 |

# High Speed CMOS Uncommitted Logic Arrays

## FEATURES

- Offers advantages of custom design without the development cost or time
- "PC board on a chip" approach allows simple, easy to design technique by customer or General Instrument
- Single mask commitment pattern
- 5ns gate delay
- Single supply voltage (3V to 6V)
- Low power dissipation due to silicon gate CMOS technology
- Available on-chip power-on reset option
- Full design package for customer designs available
- Short turnaround time, typically 6-8 weeks from layout to prototypes

## WHAT ARE GENERAL INSTRUMENT ULAs?

The General Instrument Uncommitted Logic Arrays consist of a matrix of pre-processed basic logic and peripheral cells which require only a single layer of metal interconnections to be made into a custom designed circuit

The design process consists of interconnecting, via the extensive interconnection highway, standard cells selected from the comprehensive cell library (Each standard cell being constructed from one or more basic cells) This simple procedure, which requires no special semi-conductor design experience, is similar to printed circuit board layout and may be undertaken either by the customer or by General Instrument

## ARRAY DESCRIPTION

The gate array consists of rows of basic logic cells with interconnection highways between each row On the edge of the chip, surrounding the logic cells, are basic peripheral cells with an interconnection highway between the peripheral and the logic cells The peripheral cells buffer signals into and out of the chip See Figure 1.

The customer's circuit is built up using fully characterized standard cells selected from the large, comprehensive cell library Each standard cell is constructed from one or more of the basic logic cells (or from one basic peripheral cell in the case of the standard peripheral cells)

## THE GENERAL INSTRUMENT ARRAYS

| Type No. | No. of Gates | No. of I/O Pads | Minimum Package Size |
|---|---|---|---|
| LA03 | 324 | 32 | 14 |
| LA05 | 560 | 40 | 16 |
| LA10 | 950 | 52 | 16 |
| LA15 | 1440 | 64 | 22 |
| LA20 | 2014 | 76 | 24 |

1 gate = 1 basic logic cell
= 2 N-Channel + 2 P-Channel transistors configurable as a dual inverter, 2 input NAND gate, transmission gate etc

Note: Pin count includes 2 power pins.

The cell library includes

- Simple gates (AND, OR, NAND, NOR, exclusive OR etc )
- Latches
- Decoders
- Shift Registers
- Arithmetic Elements
- Input Buffers
- Output Buffers

A complete list of standard cells appears at the end of this data sheet and includes a cross-reference to standard 4000 series CMOS integrated circuits

The interconnection between the standard cells is done in the interconnection highways, each of which can carry up to ten tracks Extensive cross-under facilities are provided in these highways to allow tracks to cross each other in order to connect to the standard cells

The metal interconnections inside standard cells are held on the General Instrument graphics system and are automatically added to the interconnections between the cells at the digitization stage

## BASIC LOGIC CELL

The basic logic cell consists of 4 MOS transistors (2 N-Channel and 2 P-Channel) connected together as shown in Figure 2

The gate connections are in polysilicon, are continuous through the cell and are available at the metal contacts both at the top and the bottom of the cell

The two P-Channel transistors each have one common source (drain) and one isolated source (drain) each of which may be connected to the metal contacts at the top of the cell

Similarly the N-Channel transistors have their source and drain at the bottom of the cell

The power supply lines are taken through every cell in metal

The internal connections of the cell (which convert the four separate transistors of one (or more) basic logic cells into a standard cell) are made in metal. See Figure 3.

The interconnections between standard cells are made to the metal contacts at the top and bottom of the cells

## BASIC PERIPHERAL CELL

The basic peripheral cell consists of an input section and an output section See Figure 4

The input section has two MOS transistors (one N- and one P-Channel) connected to form an inverter A resistor in series with the gates plus two catching diodes gives input static protection A 2kΩ and a 15kΩ pull-up resistor are available which may be, optionally, connected to the input

The output section also has two MOS transistors (one N- and one P-Channel) which may be connected to form either an open drain, totem pole or tri-state output stage Two catching diodes are provided to give output static protection

The peripheral cell also has a bonding pad which is linked, inside the cell, to the input and/or output sections and is the point to which the external bond wires to the chip are connected

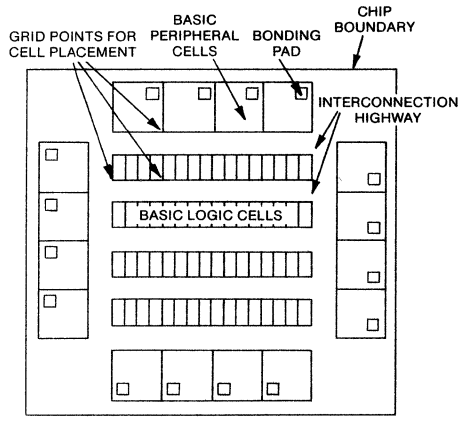



**Fig.1 BASIC GATE ARRAY LAYOUT**

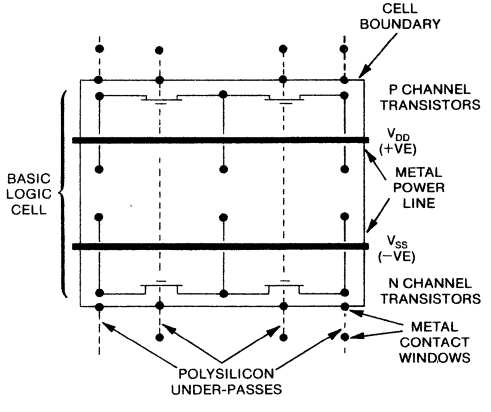



**Fig. 2 BASIC LOGIC CELL SCHEMATIC**

## INTERCONNECTION HIGHWAY

The interconnection highways between the rows of cells can accommodate up to ten tracks. See Figure 5

Connections across the highway may be made via the polysilicon underpasses as shown in Figure 5, where track 7 (marked start) is connected via the underpasses (which pass under tracks 1 to 6) to the contact window (marked end)

Connections are made between the metal tracks and the polysilicon underpasses only at the contact windows.

## DESIGN PROCESS

Designing with the General Instrument ULAs is no more complicated than designing in 4000 series CMOS or 7400 series TTL. Instead of a CMOS or TTL data book, the reference is the extensive General Instrument cell library of fully characterized logic and peripheral cells Choosing the appropriate element is as easy as looking up a CMOS catalog for the desired gate. If the design is already in standard CMOS, a quick cross-reference to the nearest equivalent in the ULA library is provided.

Once logic design is complete, the design process is reduced to one which very closely resembles a PC board layout and wiring operation. General Instrument provides a sheet of temperature-stable mylar material with the cell placement grid and polysilicon underpasses drawn on it at a scale of 250:1. A portion of the grid is shown in Fig. 6.

In addition to the grid, adhesive backed logic decals are available from General Instrument for each of the library cells. Cell placement simply involves choosing the correct decal and locating it on the grid by aligning the registration marks on the decal with those on the grid. Fig. 6 also illustrates this process and Fig. 7 shows examples of the decals. As can be seen, the decals are drawn at the logic symbol level, no transistor-level information is provided, nor is it necessary for interconnecting one cell with another. The only other information available from the decals is the position of the input and output connections. When properly aligned with the grid registration points, these inputs and outputs appear precisely at the correct polysilicon underpasses.

Interconnections between cells are made by drawing metal tracks in the spaces provided in the interconnection highway or, alternatively, placing tape between the appropriate contacts Tape of the correct width is provided in the General Instrument design package and offers a better solution than pencil since it leaves no residual marks when removed.

This "PC board on a chip" concept makes for a highly flexible design technique and one which is ideal for customer designs since MOS knowledge and transistor-level acquaintance with the array layout are not prerequisites for undertaking a design.

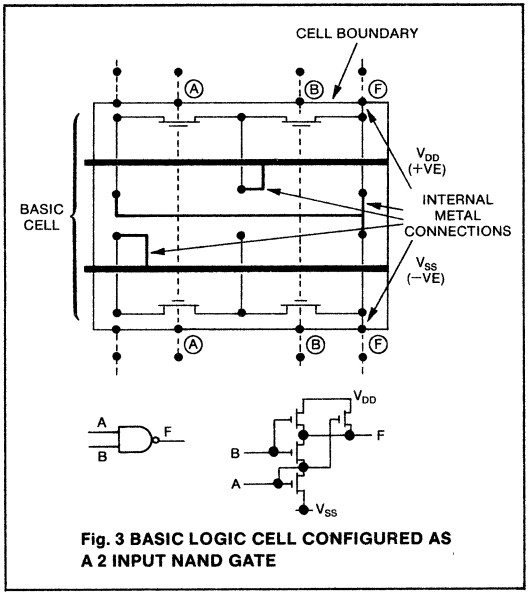



**Fig. 3 BASIC LOGIC CELL CONFIGURED AS A 2 INPUT NAND GATE**

As an alternative to the manual design method described, a Computer Aided Design (CAD) technique is available from General Instrument. This approach facilitates ease and speed of design through the use of a Calma compatible software data base containing all necessary design information.

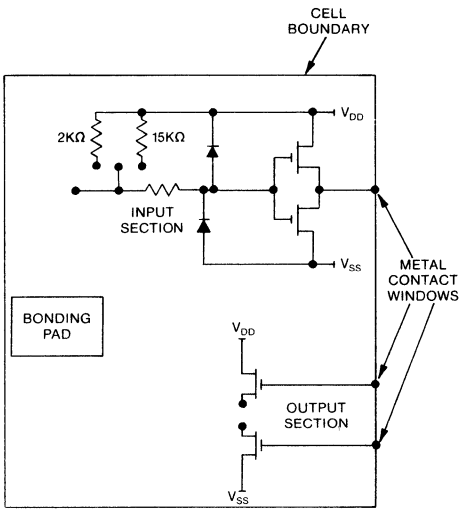



**Fig. 4 BASIC PERIPHERAL CELL SCHEMATIC**

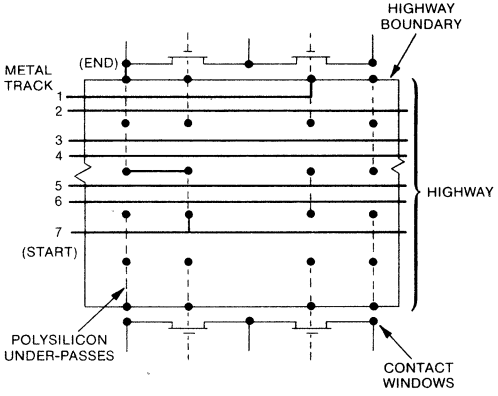



**Fig. 5 INTERCONNECTION HIGHWAY SCHEMATIC**

## CUSTOMER INTERFACES

There are three possible design routes which may be taken up to the prototype stage

I) General Instrument designs the ULA from the customer's logic diagram This interfacing route will follow the flow chart of Figure 8

II) Customer designs in ULA format as shown in Figure 9

III) Customer takes design through layout General Instrument's involvement begins at the Digitization stage prior to mask generation Figure 10 defines this design route

Variations on these basic design routes are possible in consultation with General Instrument

## AVAILABLE FROM GENERAL INSTRUMENT

1 Data sheets and brief explanation of ULA design procedures

2 Detailed specification and design manual

3 Full design package including
- Cell library of fully characterized logic elements with complete electrical specification for each cell
- Mylar layout grid
- Set of logic decals
- Interconnection tape
- Calma data base

4 Training and advice on design procedures and interpretation of logic simulation results

5 Complete design capability

## BUDGETARY QUOTATIONS

To enable General Instrument to perform a realistic appraisal of a proposed ULA design, the following information, at a minimum, must be supplied

1 A clearly defined logic diagram of the proposed ULA chip with a brief description of its operation

2 An electrical specification for important parameters including operating voltage range

3 Temperature range of operation

4 I/O definition and input/output impedances

5 Required package type

6 Proposed prototype delivery date.

7 The level of customer involvement, that is, which of the three design routes will be followed

8 Intended production volume

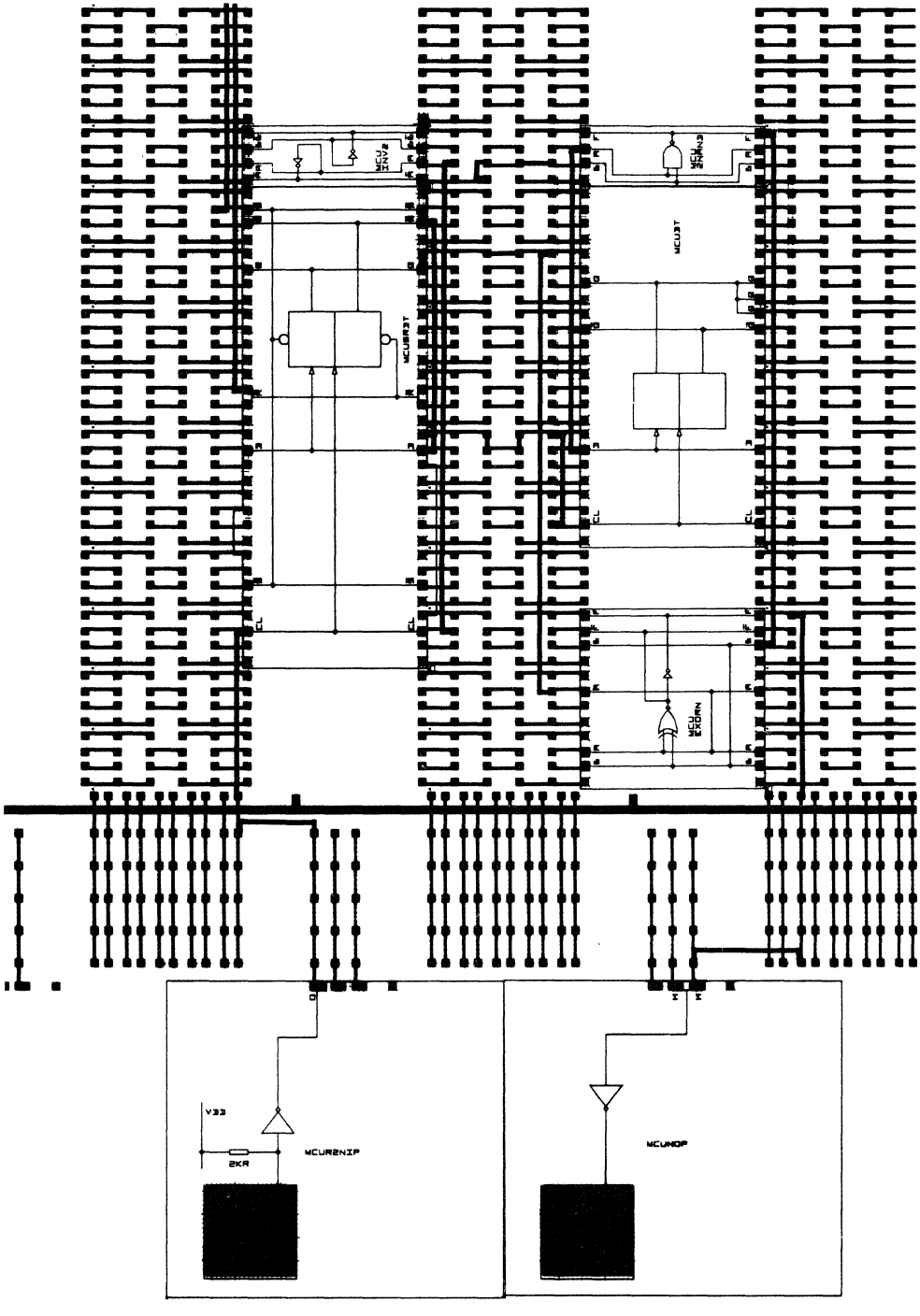
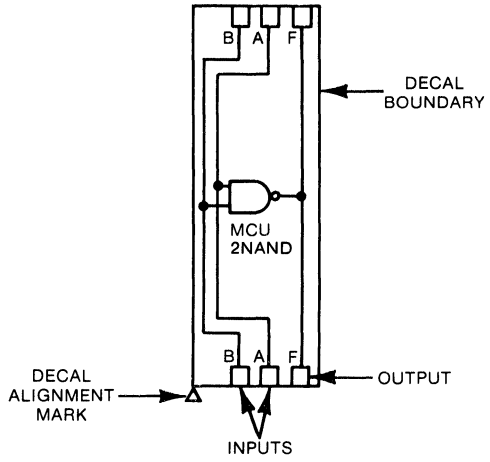
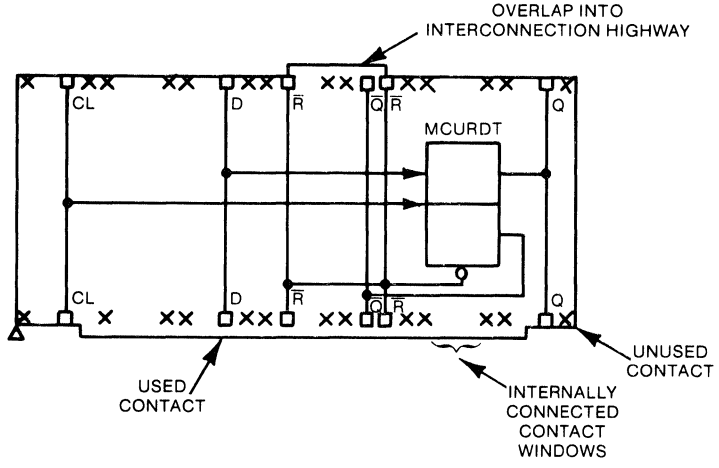



Fig. 6 SECTION OF TYPICAL LAYOUT

(a)




(b)




(c)

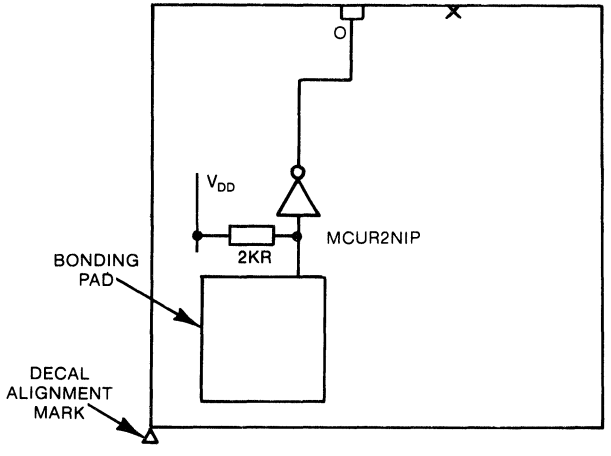



**Fig. 7 TYPICAL LAYOUT DECALS**

**PROCEDURE I GENERAL INSTRUMENT DESIGNS ULA**

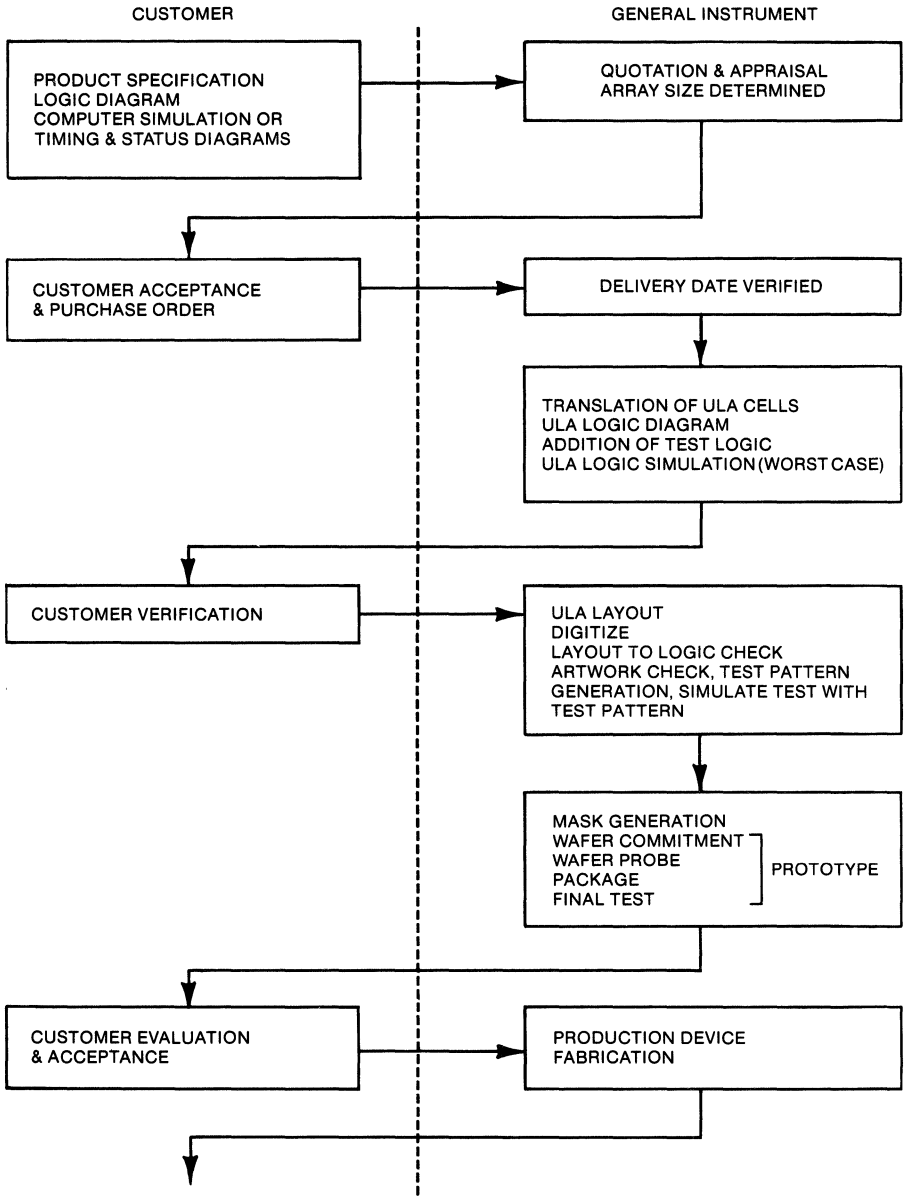



**Fig. 8 DESIGN INTERFACE**

**PROCEDURE II CUSTOMER DESIGNS IN ULA FORMAT**

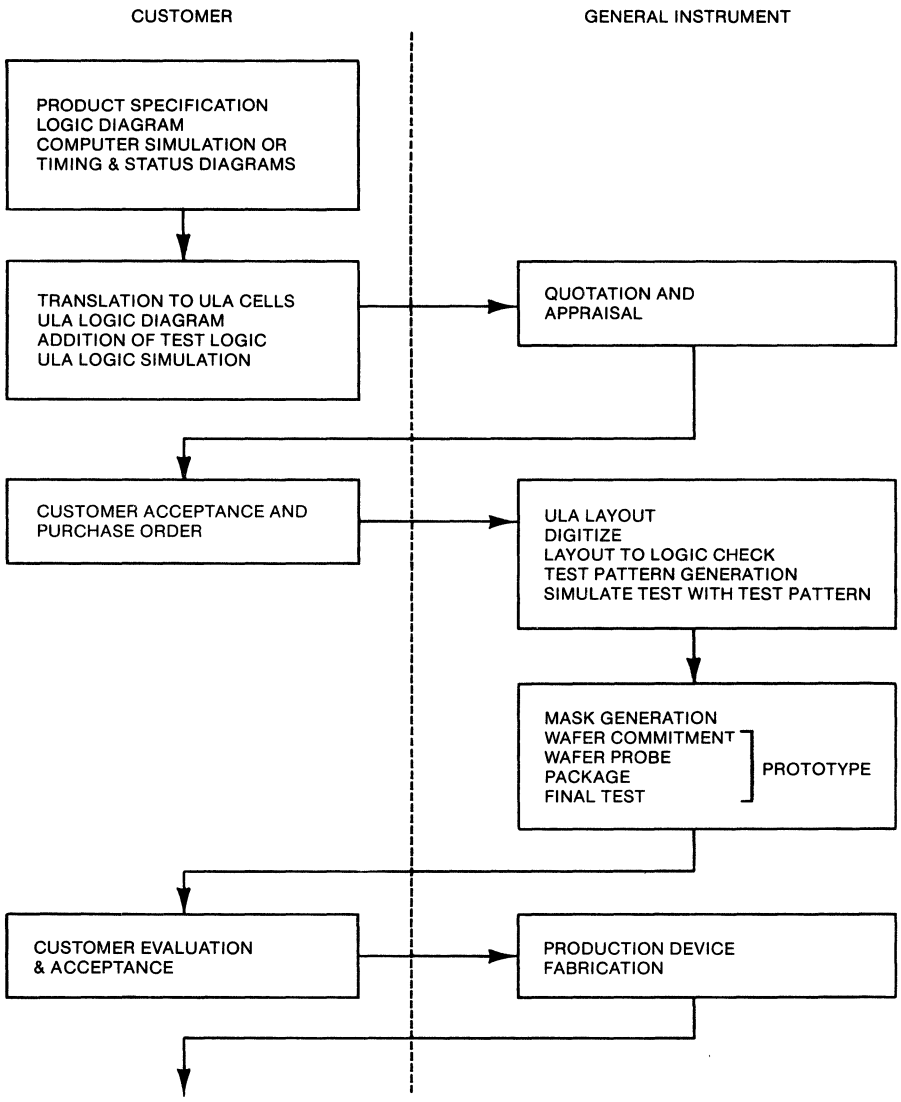



**Fig. 9 DESIGN INTERFACE**

**PROCEDURE III CUSTOMER DESIGNS ULA**

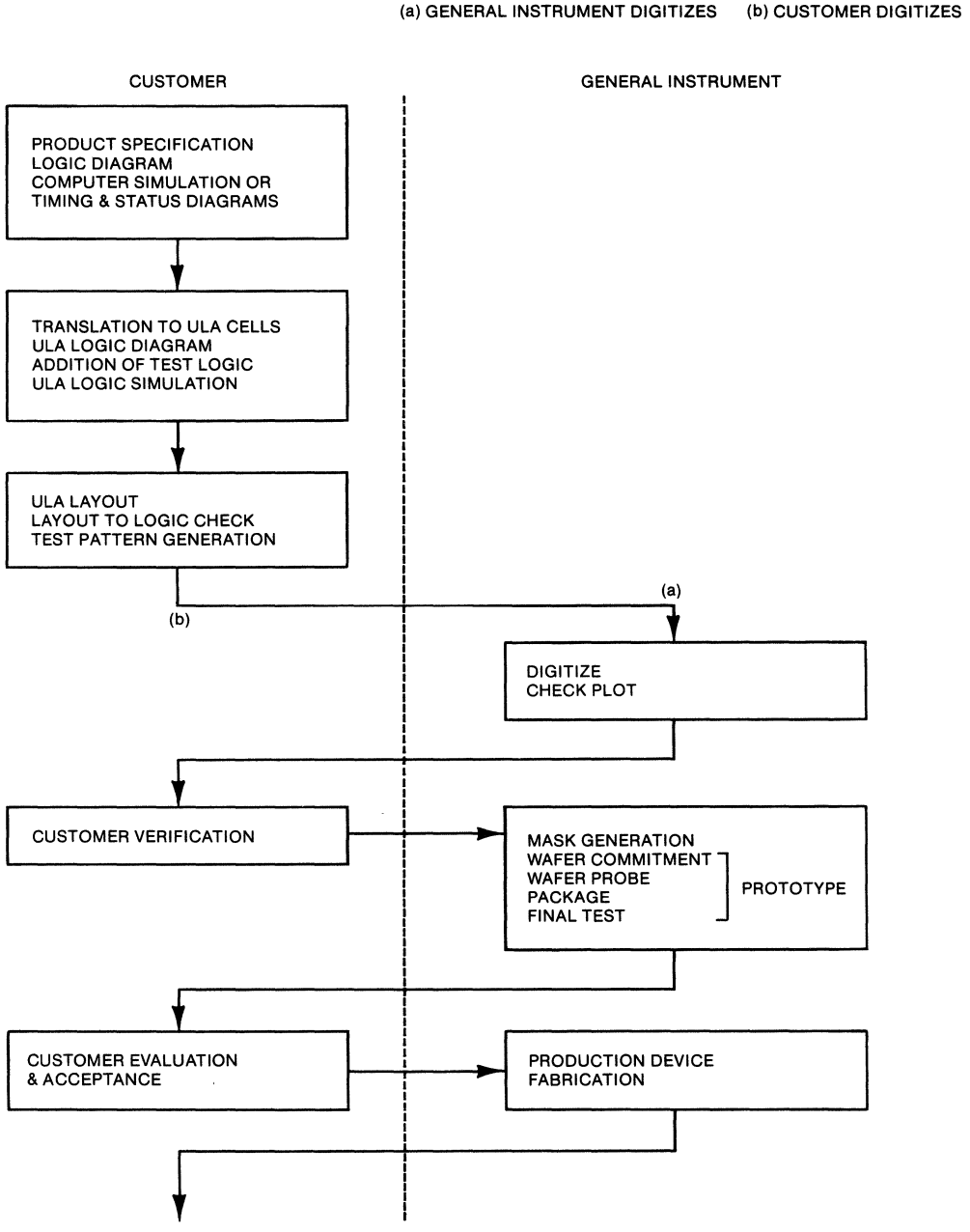



**Fig. 10 DESIGN INTERFACE**

## ELECTRICAL CHARACTERISTICS

### Maximum Ratings*

All inputs and outputs (with respect to GND) .....−0 3V to 7V
Storage Temperature ..... −65° C to +150° C
Operating Temperature ..... −55° C to +125° C
Soldering Temperature of leads (10 seconds) ..... +300° C

**Standard Conditions** (unless otherwise stated)·
Operating Voltage Range +3V to +6V
Operating Temperature Range 0° C to +70° C
−40° C to +85° C

*Exceeding these ratings could cause permanent damage to the device. This is a stress rating only and functional operation of this device at these conditions is not implied — operating ranges are specified in Standard Conditions Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Data labeled "typical" is presented for design guidance only and is not guaranteed

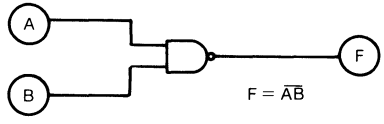


Typical gate delay at 25° C and +5V is 5ns However, the characteristics of each logic element are specified independently for each of the library cells Two examples are shown below

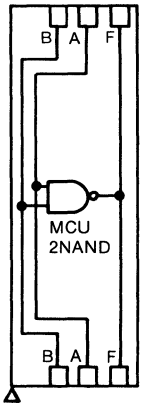
## CELL LIBRARY SPECIFICATIONS

### EXAMPLE 1:

**2 INPUT NAND GATE (MCU2NAND)**




LOGIC

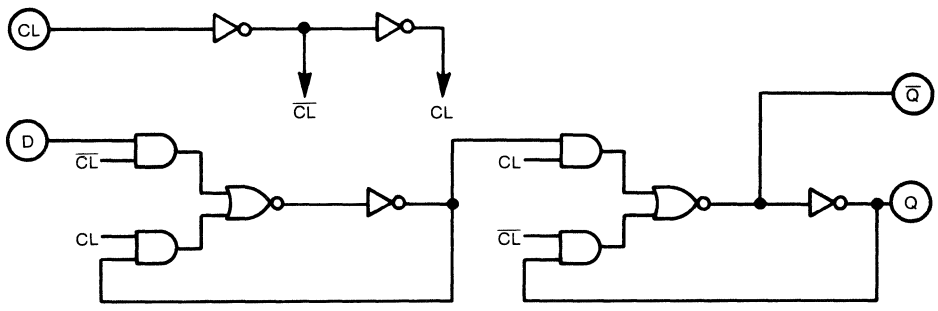



BLOCK SCHEMATIC

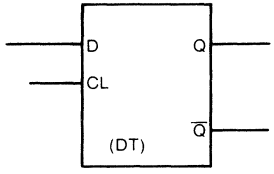
| Characteristics | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Propagation Delay Time | | | | | |
| High to Low Level | — | 0 | 0 | ns | |
| Propagation Delay Time | | | | | |
| Low to High Level | — | 0 | 0 | ns | |
| Transition Time | | | | | |
| High to Low Level | — | 4 | 5 2 | ns/pF | |
| Transition Time | | | | | |
| Low to High Level | — | 4 5 | 5 8 | ns/pF | |
| Input Capacitance | — | 35 | .5 | pF | |
| Inherent Output Capacitance | — | 7 | 9 | pF | |

**EXAMPLE 2:**
**D-TYPE FLIP-FLOP (MCUDT)**

**LOGIC**




**POSITIVE EDGE TRIGGERED FLIP-FLOP**

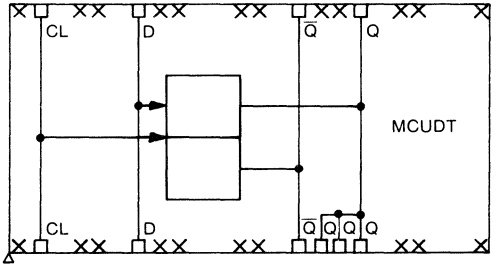



**TRUTH TABLE**

| IN | | OUT | |
|---|---|---|---|
| CL | D | Q | $\overline{Q}$ |
| ↗ | 0 | 0 | 1 |
| ↗ | 1 | 1 | 0 |
| ↘ | X | Q | $\overline{Q}$ |

NO CHANGE

**BLOCK SCHEMATIC**




| Characteristics | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|
| Propagation Delay Time: Clock to Q | — | 20 | 34 | ns | |
| Clock to $\overline{Q}$ | — | 7 | 12 | ns | |
| Transition time | | | | | Note 1 |
| High to Low Level Q | — | 2.0 | 2 6 | ns/pF | |
| $\overline{Q}$ | — | 4 0 | 5 4 | ns/pF | |
| Low to High Level Q | — | 4.5 | 5 8 | ns/pF | |
| $\overline{Q}$ | — | 9 | 11 7 | ns/pF | |
| Clock Input Frequency (Q & $\overline{Q}$ Unloaded) | dc | — | 17 | MHz | |
| Data Set Up Time | 30 | — | — | ns | |
| Data Hold Time | 12 | — | — | ns | |
| Clock Rise or Fall Time | — | — | 1000 | ns | |
| Input Capacitance. Node CL | — | 35 | 5 | pF | |
| D | — | 35 | 5 | pF | |
| Inherent Output Capacitance: Node Q | — | 85 | 1 1 | pF | Note 2 |
| $\overline{Q}$ | — | 1 35 | 1 8 | pF | |

NOTES.
1. If $\overline{Q}$ is loaded total propagation delay time to Q = propagation delay time to Q + additional transition time to $\overline{Q}$.
2. If Q or $\overline{Q}$ has to drive a switched load (eg. D input to MCUTRI) then outputs must be buffered with inverter cell.

## STANDARD CELL LIST

| Cell Description | Cell Name | No. of Gate Equivalents | Nearest CMOS Equivalent |
|---|---|---|---|
| **Gates** | | | |
| Inverter Fast | MCUINV1 | 1 | 4069 |
| Dual Inverter | MCUINV2 | 1 | 4069 |
| 21P NAND Gate | MCU2NAND | 1 | 4011 |
| 21P NAND/AND Gate + Inverter | MCU2AND | 2 | 4018 |
| 31P NAND/Gate + Inverter | MCU3NAND | 2 | 4023 |
| 31P NAND/AND Gate | MCU3AND | 2 | 4073 |
| 41P NAND Gate | MCU4NAND | 2 | 4012 |
| 41P AND/NAND Gate + Inverter | MCU4AND | 3 | 4082 |
| 21P NOR Gate | MCU2NOR | 1 | 4001 |
| 21P NOR/OR Gate + Inverter | MCU2OR | 2 | 4071 |
| 31P NOR Gate + Inverter | MCU3NOR | 2 | 4025 |
| 31P NOR/OR Gate | MCU3OR | 2 | 4075 |
| 41P NOR Gate | MCU4NOR | 2 | 4002 |
| 41P NOR/OR Gate + Inverter | MCU4OR | 3 | 4072 |
| 2 AND 2 NOR Gate | MCU2ANNO | 2 | 4085 |
| 2 AND NOR/OR Gate + Inverter | MCU2ANOR | 3 | 4019 |
| Transfer (Tri-State) Gate + Inverter | MCUTRI | 2 | 4070 |
| Exclusive OR/NOR Gate | MCUEXORN | 3 | 4077 |
| **Arithmetic** | | | |
| Half Adder + Inverter | MCUHAD | 4 | |
| Full Adder | MCUFAD | 7 | 4008 |
| **Registers & Latches** | | | |
| Set-Reset D Type Flip Flop | MCUSRDT | 8 | 4013 |
| Reset D Type Flip Flop | MCURDT | 7 | 4013 |
| Set D Type Flip Flop | MCUSDT | 7 | 4013 |
| D Type Flip Flop | MCUDT | 6 | 4013 |
| Set-Reset D Latch | MCUSRDL | 5 | |
| Reset D Latch | MCURDL | 4 | |
| Set D Latch | MCUSDL | 4 | |
| D Latch | MCUDL | 4 | 4042 |
| NOR S/R Latch | MCUNOSR | 3 | 4043 |
| NAND S/R Latch | MCUNASR | 3 | 4044 |
| D Register (First Bit) | MCUDREGF | 5 | |
| D Register (Middle Bit) Dual | MCUDREGM | 5 | 4042 |
| D Register (End Bit) | MCUDREGE | 3 | |
| Shift Register (First Bit) | MCUSHRF | 10 | |
| Shift Register (Middle Bit) | MCUSHRM | 5 | 4015 |
| Shift Register (End Bit) | MCUSHRE | 5 | |
| Half Parallel Loading Shift Reg Clock Drivers | MCUHPLSF | 8 | |
| Half Parallel Loading Shift Reg First and Middle Bit | MCUHPLSM | 7 | 4021 |
| Half Parallel Loading Shift Reg End Bit | MCUHPLSE | 7 | |
| **Decoders** | | | |
| Expandable 7-Segment Decode Segment a | MCU7SGA | 7 | |
| Expandable 7-Segment Decode Segment b | MCU7SGB | 7 | |
| Expandable 7-Segment Decode Segment c | MCU7SGC | 5 | |
| Expandable 7-Segment Decode Segment d | MCU7SGD | 8 | 4055 |
| Expandable 7-Segment Decode Segment e | MCU7SGE | 5 | |
| Expandable 7-Segment Decode Segment f | MCU7SGF | 8 | |
| Expandable 7-Segment Decode Segment g | MCU7SGG | 8 | |
| **Service Elements** | | | |
| 2 Row Interconnect | MCU2INT | 1 | |
| **Peripheral** | | | |
| Input Buffer Inverting | MCUNIP | | |
| Input Buffer Inverting with 15kΩ Pull Up Resistor | MCURINIP | | |
| Input Buffer Inverting with 2kΩ Pull up Resistor | MCUR2NIP | | |
| Output Buffer Inverting | MCUNOP | | |
| Output Buffer Inverting Open Drain | MCUODNOP | | |
| Tri-State Output Buffer plus Inverting Input Buffer | MCU3IO | | |
| Dummy Pad | MCUDUM | | |

## NOTES