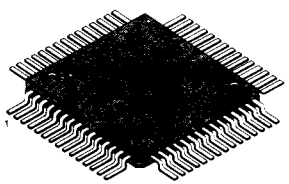
CMOS 1-CHIP SPEECH SINTHESIZER

The KS5901A is a CMOS speech synthesizer which is developed by Samsung Electronics Co. (SEC). SEC has undertaken a research & development program on an encoded reproduction algorithm called linear predictive coding (LPC). Speech is synthesized by processing an externally provided variable bit stream of LPC encoded speech data, and converting the results to the audible output with an on-chip 9 bits D/A converter.
The speech synthesis system using KS5901A is composed of the following three chips;
KS5901A : CMOS speech synthesizer
PROM : Commercial non-volatile memory (×8 bit)
Micom/μ-processor: 4/8 bits system controller (CPU mode)

With a considerable memory expansion and controller interfacing capacity, the KS5901A performs speech synthesis operation required for various applications. As the KS5901A is a CMOS LSI, the power consumption is small enough to satisfy the power specification.

60 FQP



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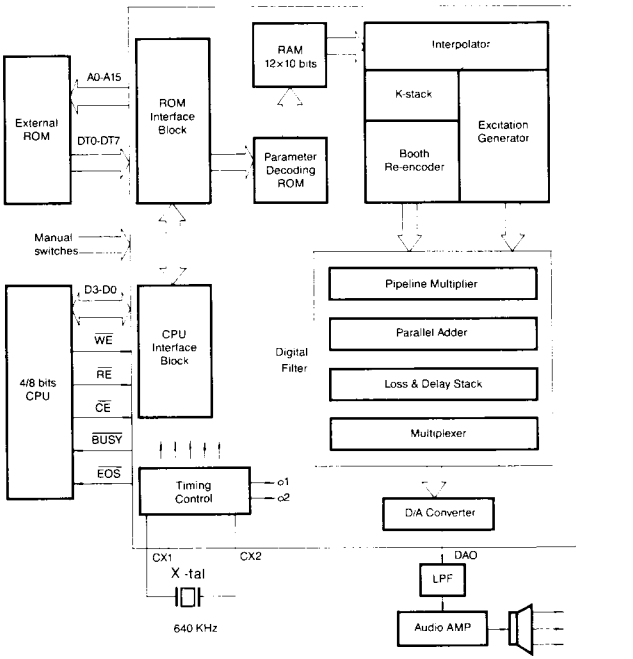
FEATURES

- **Speech synthesis method; LPC (Linear Predictive Coding)**
- **640 KHz crystal oscillation**
- **8 KHz sampling frequency**
- **Control mode; CPU control/manual control**
- **Various synthesis speed; 0.7-1.55 times of normal speed.**
- **Various speech synthesis conditions;**
  - **Excitation source**
    Voiced speech; impulse/triangular pulse
    Unvoiced speech; white Gaussian noise
  - **Bit allocation/frame**
    48 bits/frame; nonlinear transformation
    96 bits/frame; linear transformation
  - **Frame length; 10/20msec per frame**
  - **Repetition of the speech parameter set is possible.**
  - **Loss factor of the synthesis filter is controllable.**
  - **Variable stage of the digital filter; 8/10 stage.**
- **Direct access to the external ROM (×8 bit)**
- **Maximum memory size; 64K bytes**
- **Easy interface with CPU**
  - **4 bits interface bus line**
  - **12-kinds of command**
  - **Monitoring the 4 kinds of status flags**
  - **$\overline{\text{BUSY}}$, $\overline{\text{EOS}}$ (End of speech) output**
  - **External ROM data dump mode**
  - **Less CPU overhead**
- **On chip 9 bits R-2R D/A converter**
- **Low power consumption due to the 2-phase CMOS structure**
- **Single +5V power supply**

BLOCK DIAGRAM



*) LPF: LOW PASS FILTER

Fig. 1 KS5901A functional block diagram

PIN CONFIGURATION

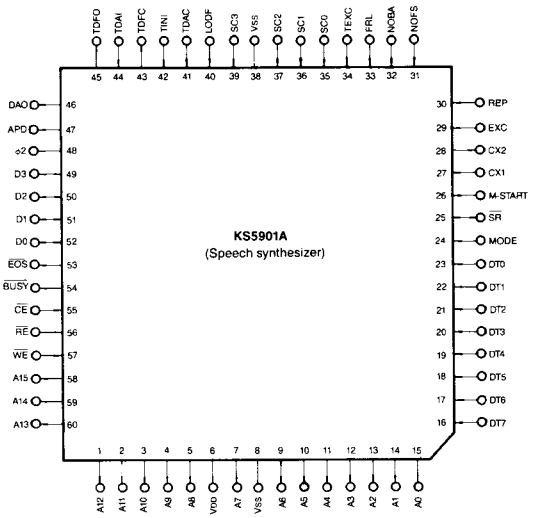


Fig. 2 Pin configuration (60 FQP top view)

PIN DESCRIPTION

Pin (No.)	Name	Input/Output	Function
$A_{15} \sim A_0$ (58-60, 1-5, 7, 9-15)	Address output	Output	Used for external PROM Interface (16 bits address line)
$DT_7 \sim DT_0$ (16-23)	Data input	Input	Used for speech data input from external PROM (8 bit data line)
MODE (24)	Mode switch	Input	Selects CPU or manual control mode H: CPU control L: manual control
$\overline{SR}$ (25)	System reset	Input/Output	System reset. Clears internal registers. (active low)
M-START (26)	Manual start	Input	In the manual control mode, M-START signal initiates reading of external ROM data, starting the synthesis operation.
CX1 (27) CX2 (28)	Oscillator	Input Output	Pins for connecting crystal oscillator
EXC (29)	Excitation source	Input	H: Triangular pulse L: Impulse
REP (30)	Parameter repetition	Input	H: Without repetition L: With repetition
NOFS (31)	Number of filter stages	Input	H: 8-stages L: 10 stages
NOBA (32)	Number of bit allocation	Input	H: 96 bits/frame L: 48 bits/frame
FRL (33)	Frame length	Input	H: 10 msec/frame L: 20 msec/frame
LODF (40)	Loss of digital filter	Input	H: With Loss L: Without Loss
			(In the manual control mode, these pins must be selected to "H" or "L" according to the synthesis conditions.
TEXC (34) TDAC (41) TINI (42) TDAI (44)	Test	Input	Pins for LSI Test (normally ground)
TDFC (43) TDFO (45)	Test	Output	Pins for LSI test (these pins should be open.)
$SC_3 \sim SC_0$ (39, 37-35)	Speed select	Input	In the manual control mode, the synthesis speed follows the "H"/"L" combination of SCO-SC3. Synthesis speed is varied from 0.7 to 1.55.
DAO (46)	D/A output	Output	9 bits R-2R D/A converter output
APD (47)	Audio power down	Output	Controls the power of external audio circuit
$\phi 2$ (48)	System clock	Output	160 KHz system clock output

(continued)

Pin (No.)	Name	Input/Output	Function
$D_3 \sim D_0$ (49-52)	CPU interface bus	Input/Output	Used for CPU interface. When $\overline{WE}$ and $\overline{CE}$ are set to low, these pins are used for command input. When $\overline{RE}$ and $\overline{CE}$ are set to low, these pins are used for monitoring the status flags or reading external ROM data. When $\overline{CE}$ is high, these are in tri-state.
$\overline{EOS}$ (53)	End of speech	Output	When the synthesis operation is terminated by END1 code, $\overline{EOS}$ output is set to low level during one frame. (10/20 msec)
$\overline{BUSY}$ (54)	Busy output	Output	In the CPU control mode, Busy signal is generated by $\overline{WE}$/$\overline{RE}$ or Osc. enable. (active low)
$\overline{CE}$ (55)	Chip enable	Input	Enables the KS5901A to accept command from CPU during $\overline{WE}$ or to transmit data to CPU during RE pulse. (active low)
$\overline{RE}$ (56)	Read enable	Input	If $\overline{RE}$ is active, CPU can read the LSI, (active low)
$\overline{WE}$ (57)	Write enable	Input	If $\overline{WE}$ is active, CPU can write to the LSI, (active low)
V_{SS} (8, 38)	Power	Input	Ground input
V_{DD} (6)	Power	Input	Supply voltage input (+5V)

(Tab. 1. KS5901A pin description)

*)"H" or high is 5V
"L" or Low is 0V

FUNCTIONAL DESCRIPTION

CPU control mode

When MODE pin is set to "H", the KS5901A switched into the CPU control mode in which the general micom/μ-processor can control the speech synthesizer. The KS5901A supports the 12 commands which make it possible to control the operation and synthesis conditions. It also provides 4 kinds of status flags which represent internal status of KS5901A. Thus, this mode provides the great flexibility for many applications of KS5901A.

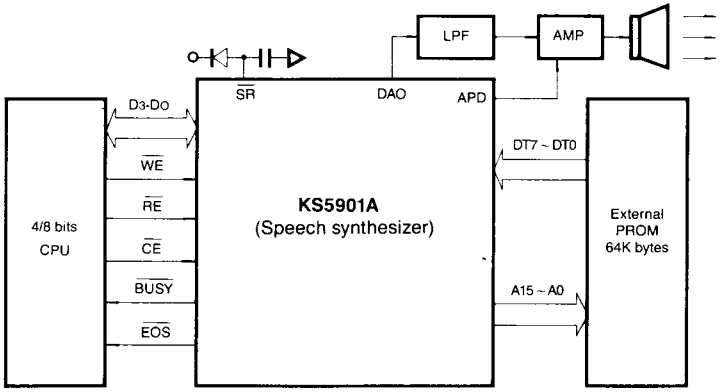


Fig. 3 System configuration in the CPU control mode

1. Commands of KS5901A

A. One nibble commands

(1) ODIS (Oscillator DISable)

This command is used to disable the internal clock oscillation of KS5901A. If the command is given, APD output and status flag of D1 (see 8 page) are set to "H", and the address counter is set to 0000H, and condition values are all cleared, and then KS5901A is turned into the reset state, as $\overline{SR}$ outputs "L" level.

(2) OENA (Oscillator ENAble)

This command releases the ODIS state and resets status flag of D1. After this command, the KS5901A becomes power-on transient state during about 40msec and the $\overline{BUSY}$ outputs the "L" level during that period. As APD output remains "H" level, AENA command should be given so as to enable the external audio circuit.

(3) ADIS (Audio DISable)

If this command is given, APD output is set to "H" level. This command is used to control the power of external audio circuit.

(4) AENA (Audio ENAble)

If this command is given, APD output is set to "L" level. This command is used to control the power of external audio circuit.

(5) STRT (STaRT synthesis operation)

This command is used to start the synthesis operation as reading the external ROM data from where the address counter points.

(6) STOP (STOP synthesis operation)

This command controls KS5901A to stop the synthesis operation. The KS5901A is changed into the stand-by state, while it hold the address counter, the synthesis conditions, speed condition and APD state. This is used to reset "ROM data error" and "command error" status flag.

(7) DDMP (Data DuMP mode)

This command is used to set the data dump mode. In this mode the CPU can read the contents of the external ROM nibble by nibble. When CPU perform its 1st read operation under DDMP mode, 4 bits data ($b_4 \sim b_1$) of the specified address are fetched through data bus ($D_3 \sim D_0$). 2nd read operation enables higher 3 bits ($b_7 \sim b_5$) and LSB 1 bit of the next address (b_0) to be dumped through $D_2 \sim D_0$ and D_3 of data bus respectively. This operation sequence can be continued, and thus the external PROM data can be read into CPU in this mode. It should be noticed that the initial LSB 1 bit (b0) at the specified address is lost because it is treated as the header bit in the KS5901A. Either the speech data or the non-speech data can be stored in the external PROM. By using this mode, the indirect addressing of speech data, i.e., label addressing method, can be carried out. (see 10 page)

(8) NOP (No OPeration)

This command has no effect on the KS5901A except releasing the data dump mode.

(9) Extra command

The KS5901A is not influenced by this command, however the "command error" flag is set to "H" level.

B. Two nibbles commands

(1) LDSPD (LoaD SPeeD code)

This command specifies the synthesis speed with 4 bits data followed by. (refer to Table 6)

(2) LDCON1 (LoaD CONdition 1)

This command specifies the conditions such as the bit allocation per frame, the frame length, the parameter repetition and the stages of digital filter with the successive 4 bits data. (refer to Table 4)

(3) LDCON2 (LoaD CONdition 2)

This command specifies the type of excitation source, the loss factor of the synthesis filter with the successive 4 bits data.

C. Six nibbles command

(1) LDADR (LoaD ADdResses)

The command specifies the start address of the phrase to be synthesized or the PROM data to be read by data dump mode with the successive 5 nibbles data which follow the LDADR command. (refer to page 10)

D. Notice

If any command is given to the KS5901A, the command execution is started between the rising edge of the $\overline{WE}$ signal and internal busy (IBUSY-see page 259) duration. Fig. 4 and 5 illustrate the timing diagrams associated with the command execution and the synthesis operation.

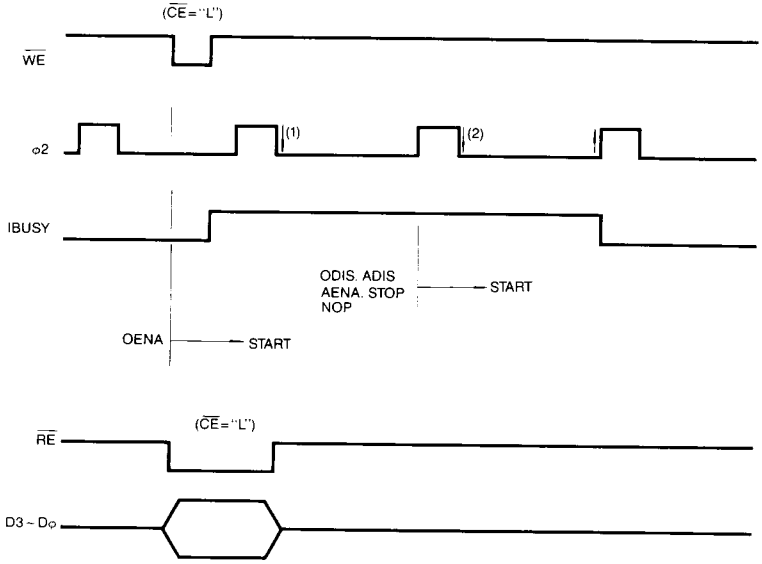


Fig. 4 Timing diagram of the execution of commands

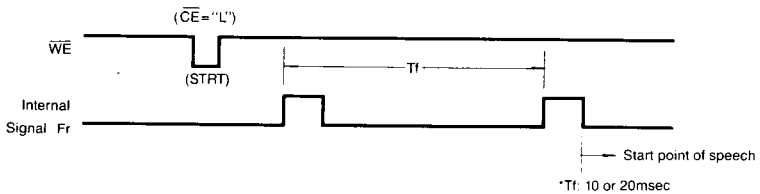


Fig. 5 Timing diagram of the synthesis operation

	Mnemonic	Code Format	Operation	IBUSY Duration
1 nibble Command	ODIS	1001	Oscillator disable, Reset.	3 T max.*
	OENA	1011	Oscillator enable.	3 T max.*
	ADIS	1010	Audio power off. (APD: H)	3 T max.*
	AENA	0100	Audio power on. (APD: L)	3 T max.*
	DDMP	1000	Set data dump mode	10 T max.
	STRT	0001	Start synthesis operation	3 T max.
	STOP	0010	Stop synthesis operation	3 T max.
	NOP	0000	No operation.	3 T max.
	Extra command	11XX	Extra commands	3 T max.
2 nibbles Command	LDSPD	0101, XXXX	Set speed	3 T max.
	LDCON1	0111, XXXX	Set synthesis condition 1	3 T max.
	LDCON2	0110, XX00	Set synthesis condition 2	3 T max.
6 nibbles Command	LDADR	0011 n n n n n**	Set address counter (A15 ~ A0)	3 T max.

*)T: 6.25μsec typ.
**) n: any 1 nibble data.

Tab. 2. KS5901A Commands

	Operation	–BUSY Duration	Caution
$\overline{RE}$	Reading status or ROM data. 2 nibbles, 6 nibbles mode is released.	Status read; 3T ROM data dump; 10T	No execution during IBUSY

Tab. 3 $\overline{RE}$ operation

2. Synthesis conditions and speed code

The synthesis conditions are determined according to the required quality of the synthesized speech and the memory size. The synthesis conditions and speed are specified by LDCON1, LDCON2, and LDSPD commands as previously described.

Condition		Synthesis Condition 1	Synthesis Condition 2
Data bus	Data	LDCON1	LDCON2
D3	L	48 bits/frame	Excitation; Impulse
	H	96 bits/frame	Triangular pulse
D2	L	20 msec/frame	Without loss effect
	H	10 msec/frame	With loss effect
D1	L	Parameter; repetition	Not used
	H	no repetition	Always "L"
D0	L	Filter stages: 10 stages	Not used
	H	8 stages	Always "L"

Tab. 4. Synthesis conditions code

Table 5 and 6 illustrate the data bit-rates associated with the synthesis conditions, and the synthesis speed corresponding to each code.

Bit Allocation	Frame Legnth	Parameter Repetition	Bit Rate (Kbps)
48 bits/frame	20msec/frame	Yes	≈ 2.4
48 bits/frame	20msec/frame	No	
48 bits/frame	10msec/frame	Yes	≈ 4.8
48 bits/frame	10msec/frame	No	
96 bits/frame	20msec/frame	Yes	≈ 4.8
96 bits/frame	20msec/frame	No	
96 bits/frame	10msec/frame	Yes	≈ 9.6
96 bits/frame	10msec/frame	No	

Tab. 5. Synthesis conditions and bit rate

Data bus HEX data	Speed rate	Data bus HEX data	Speed rate
0	1.0*	8	1.4
1	0.7	9	1.5
2	0.8	A	1.55
3	0.9	B	1.0
4	1.0	C	1.0
5	1.1	D	1.0
6	1.2	E	1.0
7	1.3	F	1.0

*Original speed = 1.0

Tab. 6. Speed control code

3. Internal status flags.

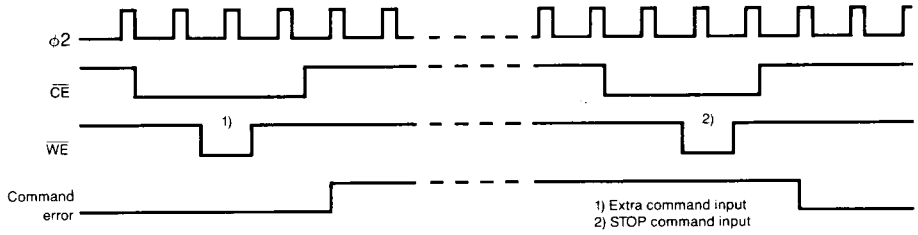
If $\overline{RE}$ signal is given under the normal operation modes except data dump mode, the 4 kinds of internal status 4 bits data bus (D3-D0) of KS5901A. Table 7 shows the summary of the internal status flags. Fig. 6 illustrates the timing associated with it's occurances.

Data Bus	Status Output	Occurance ("H")	Release ("L")
D3	Command error	• Timing error in the interface • Extra command	• Stop command • Power-on reset • Osc. disable
D2	ROM data error	• Nonexistent data • 1st frame data are all high ("I")	• Stop command • Power-on reset • Osc. disable
D1	Osc. disable	• Oscillator disable state	• Osc. enable
D0	End of speech	• Under stand-by state • Stop speech	• Under synthesis operation

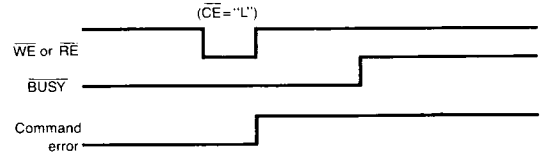
Tab. 7. Summary of the status flags

A. Command error (D3)

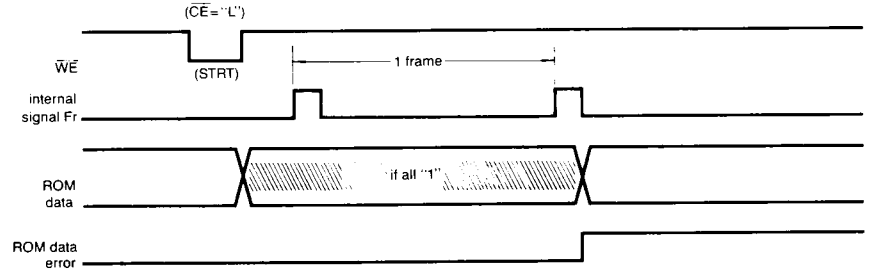
(1) Extra command input



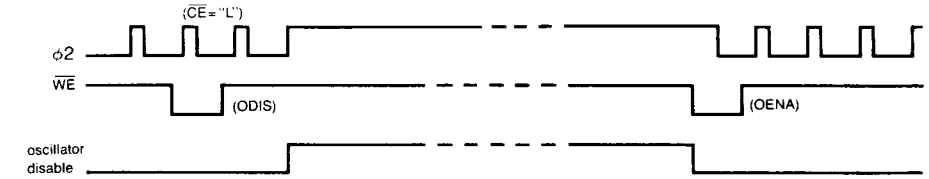
2. When BUSY is activated CE



B. ROM data error (D2)



C. Oscillator disable (D1)



D. End of speech (D0)

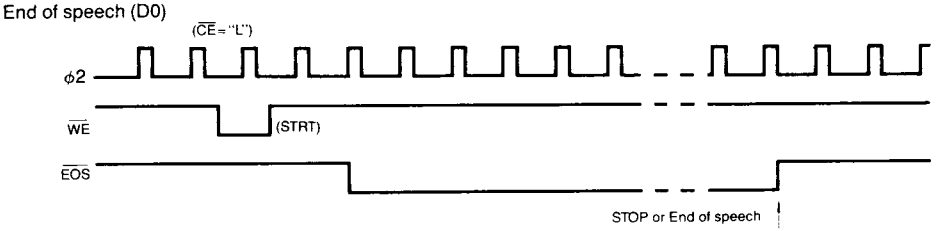


Fig. 6 Timing diagrams of the internal status flags

4. Setting the start address

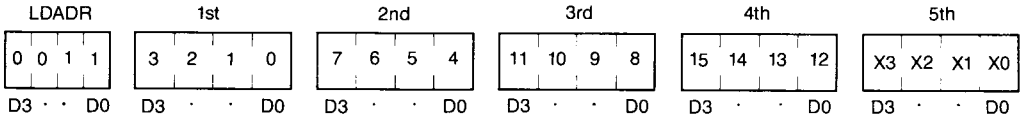
There are two ways of setting the start address of the phrase under CPU control. One is Direct addressing and the another is Indirect addressing.

A. Direct addressing

This addressing is the way to set up the start address of the phrase by directly loading the address data into the KS5901A.

* A start address is given to the 19 bits address counter by LDADR command together with the successive 5 nibbles data, of which the 5th nibble is dummy data. (see appendix)

Input format



Address in address counter

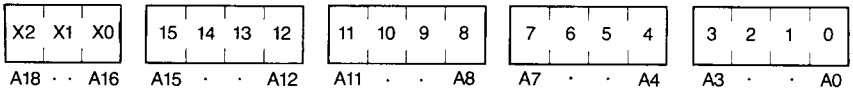


Fig. 7. ROM start address

- After loading the start address, the STRT command initiates the KS5901A to read the external ROM data and start the synthesis operation.
- The address counter continues to increase during synthesis operation until END1 code of the ROM data is detected.
- When END1 code is detected address counting is stopped and the KS5901A returns to the stand-by state.
- In stand-by state, the synthesis operation of the phrase currently addressed can be activated by STRT command
- If END2 code is detected, the start address previously specified by LDADR command is fed to the address counter, and the synthesis operation is repeated. The repetition is continued until the external control, such as STOP/ODIS command or system reset, is given.

B. Indirect addressing

In this mode, some part of speech data ROM is used to the index area. The label must be given to each phrase to be synthesized. The contents stored at the label address are used as the real start address. Address loading sequence of Indirect addressing mode is as follows.

- Using LDADR command, CPU loads the label address of the phrase to be synthesized to the address counter.
- Using DDMP command, CPU reads the start address data (3 bytes), i.e., the contents in the memory location pointed to by the label address and the next two addresses. And save then at the temporary area in the controller.
- Using LDADR command, CPU loads the real start address to the address counter of the KS5901A.
- The real start address must be stored in the format shown in Fig. 8 & 9. The LSB (b0) at the label address should be excluded in storing the start address. As the KS5901A has the addressing range of A0-A15, the last byte only contains one bit address data of A15 at the LSB (b0) and the other bits (b7 ~ b1) become dummy data. (see appendix)
- The control procedures are explained as follows. (refer Fig. 8 & 9)

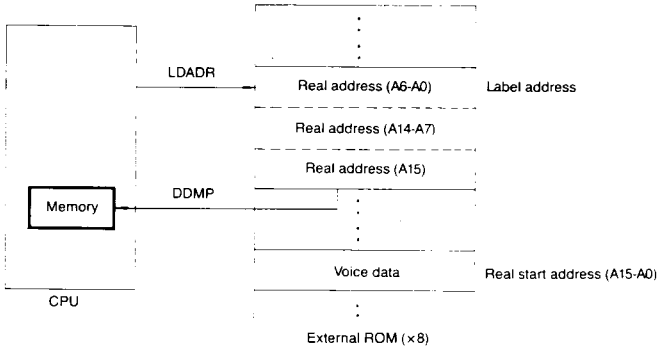


Fig. 8 Setting the label address

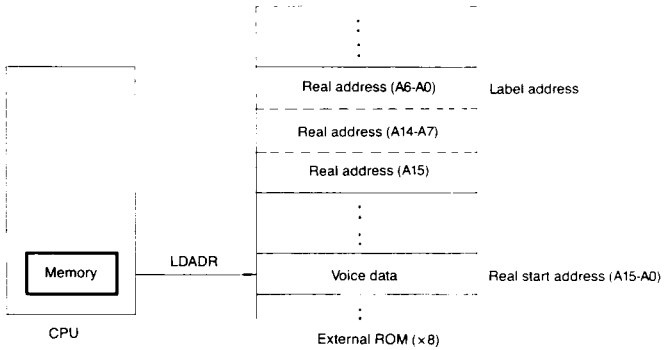


Fig. 9 Setting the real start address.

5. $\overline{\text{BUSY}}$ output

$\overline{\text{BUSY}}$ is generated in the follows:

A. During the execution time of the DDMP command and it's successive $\overline{\text{RE}}$.

$\overline{\text{BUSY}}$ is enabled during from the rising edge of the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ to the rising edge after the 9th falling of $\phi 2$. (10 T max.)

B. During the execution time of the other command or $\overline{\text{RE}}$ for status read.

$\overline{\text{BUSY}}$ is enabled during from the rising edge of the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ to the rising edge after the 2nd falling of $\phi 2$. (3 T max.) See fig. 10.

C. During power-on transient state.

Power switch ON or OENA command causes the KS5901A to be in power-on transient state, of which duration is fixed by the external capacitor connected to $\overline{\text{SR}}$ pin. In transient state. normally 40msec, KS5901A is initialized in it's internal state, and outputs $\overline{\text{BUSY}}$ signal. The $\overline{\text{BUSY}}$ signal due to OENA command become active at the falling edge of $\overline{\text{WE}}$ signal, while it is normally active at the rising edge. See Fig. 11.

* $\overline{\text{BUSY}}$ signal is available only when $\overline{\text{CE}}$ is low (Fig. 10), therefore you must hold $\overline{\text{CE}}$ to low whenever you wish to check it.
* While Internal BUSY (IBUSY) signal is active, KS5901A can not accept the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ signal.
* If the $\overline{\text{WE}}$ or $\overline{\text{RE}}$ signal is given during IBUSY signal, the internal status of the KS5901A may be uncertain. Besides, the "command error" of the status flag is set.

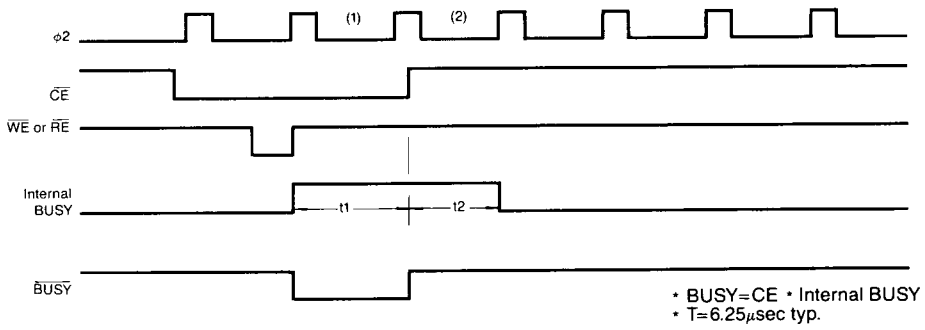


Fig. 10. Timing diagrams of BUSY signal

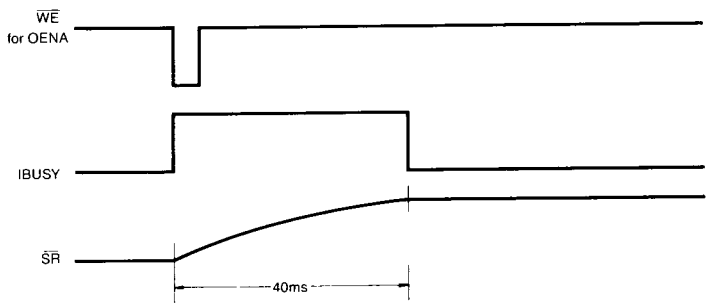


Fig. 11. Timing diagram of power-on transient state

6. Stop and restart operation

Speech synthesizing process is controlled by 2 kinds of code such as END1, END2.

A. Stop operation by END1 code

END1 code inserted at the last part of the speech parameter of a certain phrase controls the KS5901A to halt the increment of address counter, and issues EOS signal during 1 frame, remaining all it's internal condition values. At the same time status flag of D0 (End of speech) is set to high level. Figure 12 shows the timing diagram of EOS and EOS flag.

B. Restart operation by END2 code

END2 code inserted at the last part of the speech parameter of a certain phrase generates IBUSY during about 2.5ms and resets the address counter to the pre-loaded value by LDADER command, restarting synthesis operation from that address.

You can stop synthesis operation by loading STOP command in, it repeat operation without STRT command.

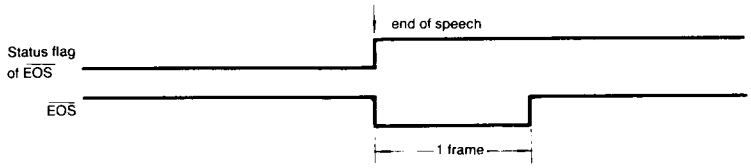


Fig. 12. Timing diagram of $\overline{EOS}$ signal

7. Notes on the CPU control mode.

A. MODE pin must be set to "L" level.
B. $\overline{BUSY}$ pin issues the output of NAND logic of the internal busy and $\overline{CE}$ signal, therefore $\overline{BUSY}$ is not issued when $\overline{CE}$ is high level.
C. $\overline{RE}$ or $\overline{WE}$ signal is not detected during internal busy singal.
D. The APD signal set to "H" by the ODIS command is not changed by the OENA command (i.e., remains "H" level). Therefore, if APD is used to control the power of external audio circuit, the AENA command must be beforehand with the START command.
E. In the CPU controlled mode the default values of conditions after reset operation are such as;
   APD : High
   Speed code : ϕH (normal speed)
   COND1 code : ϕH (48 bit, 20msec, with repetition, 10 stages)
   COND2 code : ϕH (impulse, without loss)
F. The internal status of the KS5901A is usually read by $\overline{RE}$ signal. If you want to dump the speech ROM data, DDMP mode must be set previously.
G. In the DDMP mode the 100μsec of time interval is needed at least between each read operation to dump ROM data.
H. While the synthesis operation is executed by the KS5901A, such commands as DDMP, START, 2 & 6 nibble one are forbidden.
I. After the ODIS command, the time interval of about 40msec is needed so as to execute the OENA command.

5

Manual control mode

When MODE pin is set to "L", the KS5901A is turned into the manual control mode. In this mode, all the synthesis operation and conditions can be controlled by the external switches.

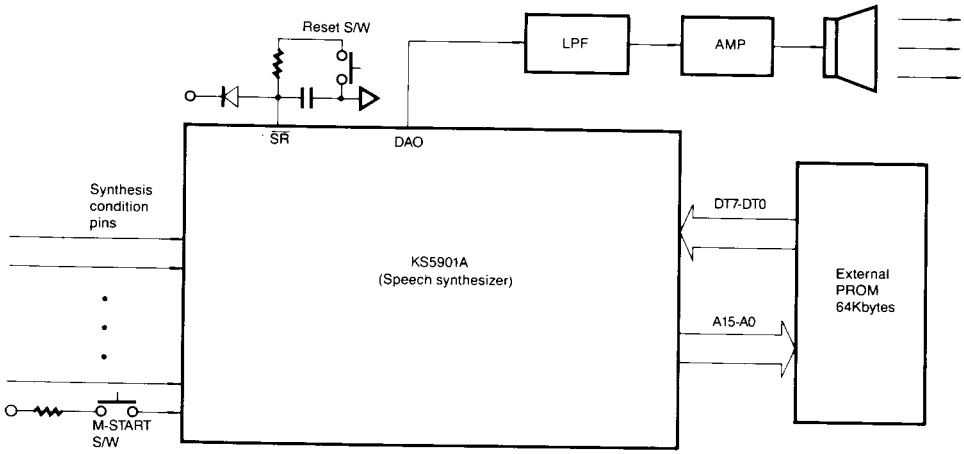


Fig. 13. System configuration the in manual control mode

1. Operation method

A. MODE pin must be set to "L" level.
B. Reset the KS5901A by means of depressing $\overline{SR}$ switch.
C. Through 10 synthesis condition pins, the synthesis conditions of the phrase to be synthesized must be specified.
D. The synthesis operation is started by means of depressing M-START switch.
E. The synthesis operation is halted by END 1 code.
F. The synthesis operation is repeated by END2 code.
G. When speech is halted by END1 code you may do the steps of C & D to perform the synthesis operation of the next phrase.
H. If you want the first phrase, you must operate the steps of B, C, D.

2. RESET operation

When Reset switch connected to $\overline{SR}$ pin is depressed or the power switch is on, the KS5901A remains the initialized state during about 40msec due to the charging time of the external capacitor attached to SR pin. M-START input is not received during that period.

3. START operation

In manual control mode, the chattering-preventing circuit is inserted to debounce the chatterings of the M-START pin. So, M-START input should be continued about min. 20msec (refer to Fig. 14)

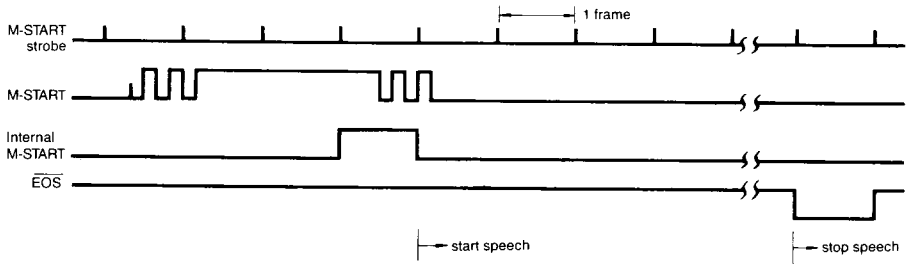


Fig. 14. Timing diagram of debouncing of the M-START signal

4. Synthesis conditions and speed.

In manual control mode, synthesis conditions are determined according to "H/L" combination of synthesis condition pins as shown bellow and synthesis speed follows the "H/L" combination of SC0-SC3 as shown in Tab. 9

Pin No.	Pin Name	Level	Synthesis Condition
29	EXC	L H	Impulse Triangular pulse
40	LODF	L H	With loss effect Without loss effect
31	NOFS	L H	Filter stages: 10 stages 8 stages
32	NOBA	L H	48 bit/frame 96 bit/frame
33	FRL	L H	20 msec/frame 10 msec/frame
30	REP	L H	Parameter: repetition no repetition

Tab. 8 Synthesis conditions in the manual control mode

Pin number				Speed	Pin number				Speed
39	37	36	35		39	37	36	35	
L	L	L	L	1.0*	H	L	L	L	1.4
L	L	L	H	0.7	H	L	L	H	1.5
L	L	H	L	0.8	H	L	H	L	1.55
L	L	H	H	0.9	H	L	H	H	1.0
L	H	L	L	1.0	H	H	L	L	1.0
L	H	L	H	1.1	H	H	L	H	1.0
L	H	H	L	1.2	H	H	H	L	1.0
L	H	H	H	1.3	H	H	H	H	1.0

*Original speed = 1.0

Tab. 9 Speed table in the manual control mode

LPC-PARAMETER EXTRACTION FLOW

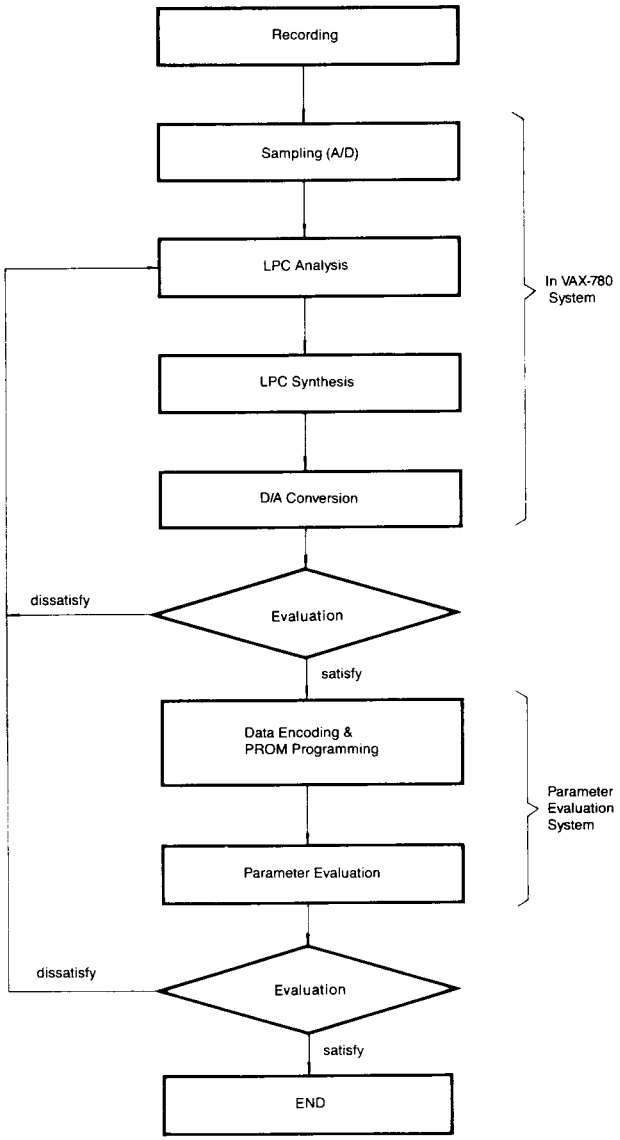


Fig. 15 LPC-parameter extraction flow

SYSTEM CONFIGURATION

1. CPU control mode

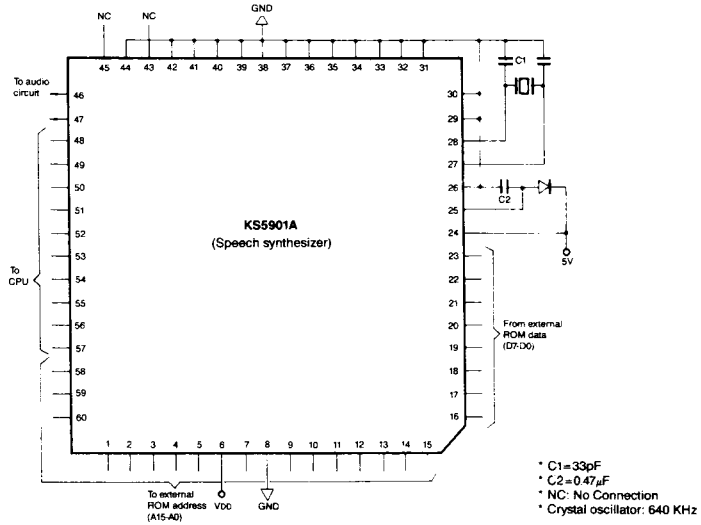


Fig. 16 System configuration in the CPU control mode

2. Manual control mode

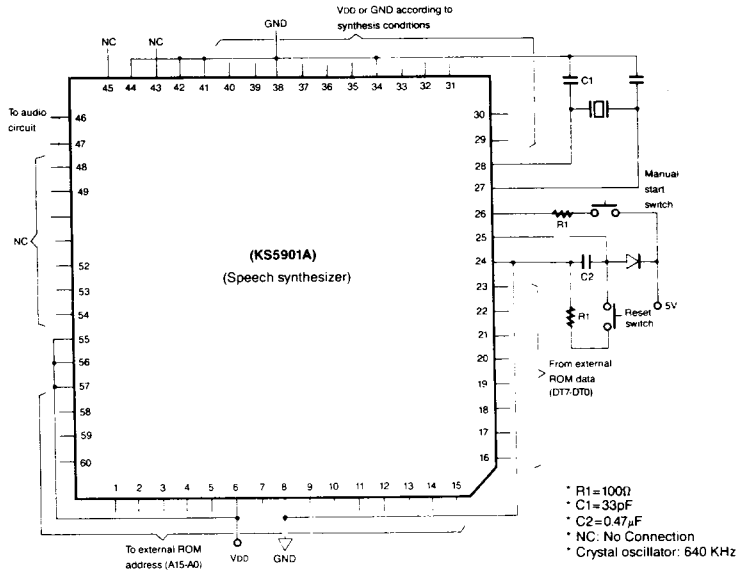
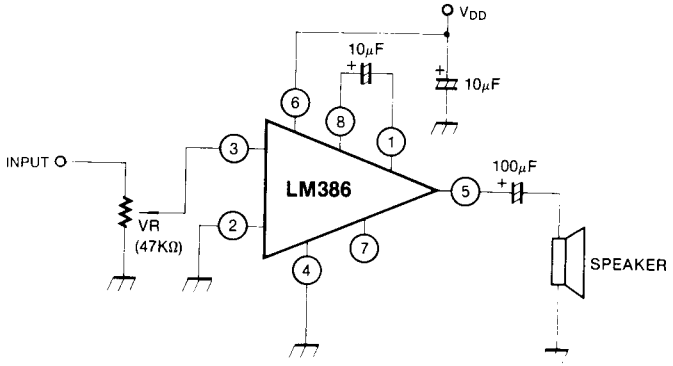


Fig 17 System configuration in the manual control mode

AUDIO CIRCUIT



ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

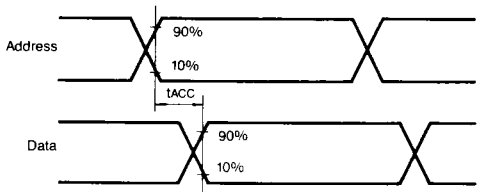
Symbol	Description	Specifications	Unit
V_{DD}	Power supply	−0.3 ~ +7.0	V
V_{IN}	Input voltage	−0.3 ~ V_{DD} + 0.3	V
T_{ST}	Storage temperature	−55 ~ +125	°C
T_{OP}	Operation temperature	−10 ~ +55	°C

Tab. 10 Absolute maximum ratings

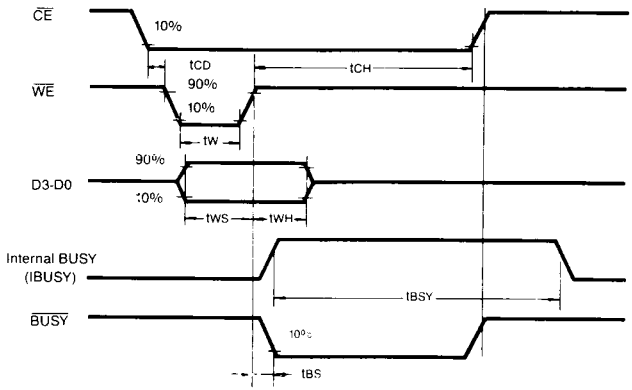
ELECTRICAL CHARACTERISTICS

Symbol	Characteristics	Conditions	Min.	Typ.	Max.	Unit
t_{CD}	Chip enable setup time	V_{DD} = 5V	200	—	—	nsec
t_W	Write enable pulse width	V_{DD} = 5V	500	—	—	nsec
t_{CH}	Chip enable hold time	V_{DD} = 5V	200	—	—	nsec
t_{WS}	Data setting time	V_{DD} = 5V	500	—	—	nsec
t_{WH}	Data hold time	V_{DD} = 5V	300	—	—	nsec
t_{BS}	Busy setting time	V_{DD} = 5V	—	—	300	nsec
t_R	Read enable pulse width	V_{DD} = 5V	1	—	—	μsec
t_{RS}	Data settling time	V_{DD} = 5V	—	—	500	nsec
t_{RH}	Data hold time	V_{DD} = 5V	—	—	500	nsec
t_{ACC}	ROM data access time	V_{DD} = 5V	—	—	1.5	μsec

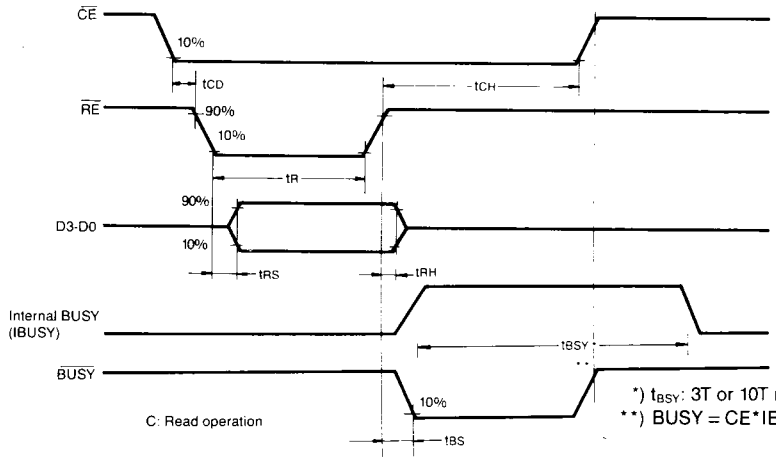
Tab. 11 AC Characteristics



A. External ROM Interface



B. Write operation



C: Read operation

*) t_{BSY}: 3T or 10T max.
**) BUSY = CE*IBUSY (see page 259)

Fig. 18 A.C. Characteristics

Symbol	Characteristics	Specific Pin	Condition	Min.	Typ.	Max.	Unit
V_{DD}	Power supply voltage	V_{DD}		4	5	6	V
I_{DDA}	Operating current	V_{DD}	V_{DD}=5V	—	1.0	1.5	mA
I_{DDB}	Stand-by current	V_{DD}	V_{DD}=5V	—	0.7	1.0	mA
I_{DDC}	Osc. disable current	V_{DD}	V_{DD}=5V	—	1.0	5.0	μA
$f\phi$	System clock frequency	ϕ2	V_{DD}=5V	155	160	165	kHz
f_{OSC}	Oscillator frequency	CX2	V_{DD}=5V	622	640	659	kHz
V_{IH}	"H" input voltage	Except $\overline{SR}$	V_{DD}=5V	V_{DD}-0.8	—	V_{DD}	V
V_{IL}	"L" input voltage	Except $\overline{SR}$	V_{DD}=5V	0	—	0.8	V
V_{OH}	"H" output voltage	Except $\overline{SR}$, DA0, CX2	No load	V_{DD}-0.4	—	V_{DD}	V
V_{OL}	"L" output voltage	Except $\overline{SR}$, DA0, CX2	No load	0	—	0.4	V
V_{OUT}	DAO output voltage	DA0	No load	0	—	V_{DD}	V
R_{INH}	Pull up resistor	$\overline{CE}$, $\overline{WE}$, $\overline{RE}$		190	380	570	kΩ
R_{INL}	Pull down resistor	M-START		70	140	210	kΩ
R_{OUT}	DAO output impedance	DAO		10	15	20	kΩ
I_{OHA}	"H" output current	A0-A15	Vout=V_{DD}-0.4	0.4	—	—	mA
I_{OHB}	"H" output current	D0-D3	Vout=V_{DD}-0.4	0.2	—	—	mA
I_{OHC}	"H" output current	$\overline{EOS}$, $\overline{BUSY}$	Vout=V_{DD}/2	1.0	—	—	mA
I_{OHD}	"H" output current	Others	Vout=V_{DD}-0.4	0.1	—	—	mA
I_{OLA}	"L" output current	A0-A15	Vout=0.4V	0.2	—	—	mA
I_{OLB}	"L" output current	D0-D3	Vout=0.4V	1.3	—	—	mA
I_{OLC}	"L" output current	$\overline{EOS}$, $\overline{BUSY}$	Vout=0.4V	1.0	—	—	mA
I_{OLD}	"L" output current	Others	Vout=0.4V	0.6	—	—	mA
I_{IH}	"H" input current	Except M-START	Vin=V_{DD}	—	—	1	μA
I_{IL}	"L" input current	Except M $\overline{CE}$ $\overline{WE}$, $\overline{RE}$	Vin=GND	—	—	1	μA

Tab. 12 D.C. characteristics

APPENDIX

KS5901A is originally designed to have 64 pins. KS5901A is the another version to replace the 64 pin package type, named KS5901. Therefore, the KS5901A is equal to the KS5901 except that it's 5 pins are excluded.

KS5901 has 19 address lines which enable it to access upto 0.5 Mbytes of external PROM/EPROM. It's internal address counter is also 19 bits wide, and you must load 1 dummy nibble to set the start address when using the KS5901A. (see page 10)

KS5901 has two more signal named PD, TINT. PD represents the status of the internal oscillator which is the same as status flag of D1. TINT is for test only.

The differences between the two chips are summarized as follows.

Item \ Device	KS5901A	KS5901
Pin count	60	64
Package type	FQP	SDIP
No. of address pin	16	19
Addressing range	64 Kbytes	0.5 Mbytes
Maximum synthesizing time	4-5 min.	40 min.